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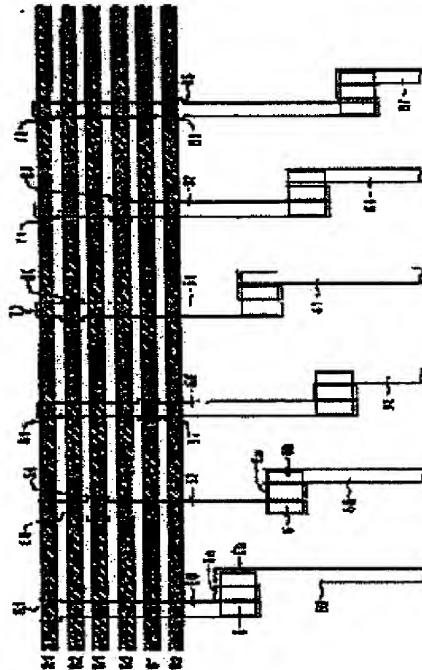
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(54) ACTIVE MATRIX TYPE DISPLAY DEVICE

(57) Abstract:

PROBLEM TO BE SOLVED: To eliminate degradation in display quantity caused by difference in signal delay for each drain line due to difference in the locations of the cross points of data signal lines 7 and drain lines.

SOLUTION: A capacitive line, which does not contribute to data transmission, is provided on a drain line to make the superimposed area with a data line to be made equal for each drain line. Thus, parasitic capacitance caused by the data line 7 and the drain line is made equal for each drain line, the difference in signal delay for each drain line is eliminated and the display quality is improved.



LEGAL STATUS

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CLAIMS

[Claim(s)]

[Claim 1] The viewing area by which two or more pixel electrodes have been arranged, and two or more data signal lines arranged at the periphery of said viewing area, Two or more drain wires which are connected to any one of said two or more data signal lines, respectively, and extend to said viewing area, In the active-matrix mold display which has two or more gate lines which intersect said two or more drain wires, and extend in said viewing area said two or more drain wires The active-matrix mold display characterized by extending so that at least one of said two or more data signal lines may be intersected in addition to the data signal line to which the drain wire was connected.

[Claim 2] Said all drain wires are active-matrix mold displays according to claim 1 characterized by having the part which intersects all data signal lines other than the data signal line to which the drain wire was connected.

[Claim 3] The area of the part to which each of said drain wire intersects said data signal line is a active-matrix mold display according to claim 2 which is in parenchyma etc. by carrying out in said all drain wires, and is characterized by things.

[Claim 4] It is the active-matrix mold display according to claim 3 which the drain wire selection switching element for choosing two or more of said drain wires as the position of the part prolonged toward said viewing area from the location connected with the data-signal line by which two or more of said drain wires correspond intervenes, and parenchyma etc. is in the distance from the location connected with the data-signal line by which two or more of said drain wires correspond to said drain wire selection switching

element by carrying out mutually with two or more of said drain wires, and is characterized by things.

[Claim 5] The viewing area by which two or more pixel electrodes have been arranged, and two or more data signal lines arranged in parallel mutually at the periphery of said viewing area, In the active-matrix mold display which has two or more gate lines which are connected to any one of said data signal lines, respectively, intersect two or more drain wires which extend to a viewing area, and said drain wire, and extend in a viewing area The part prolonged toward said viewing area from the location connected with the data signal line by which said some of two or more drain wires [at least] correspond, Have the part which keeps away from said viewing area and is prolonged, and data signal lines other than the data signal line to which the drain wire is connected in one [at least] part are intersected. The sum of the area which the drain wire and data signal line in each crossing superimpose is a active-matrix mold display which is in parenchyma etc. by carrying out with said each of two or more drain wires, and is characterized by things.

[Claim 6] For the part prolonged toward said viewing area from the location connected with the data signal line by which said two or more drain wires correspond, and the part which keeps away from said viewing area and is prolonged, the number with which it is the same size substantially and said drain wire and said data signal line cross is a active-matrix mold display according to claim 5 which is up to said two or more drain wires, and is characterized by the equal thing.

[Claim 7] It is the active-matrix mold display according to claim 6 which the drain wire selection switching element for choosing two or more of said drain wires as the position of the part prolonged toward said viewing area from the location connected with the data-signal line by which two or more of said drain wires correspond intervenes, and parenchyma etc. is in the distance from the location connected with the data-signal line by which two or more of said drain wires correspond to said drain wire selection switching element by carrying out mutually with two or more of said drain wires, and is characterized by things.

[Claim 8] The part prolonged toward said viewing area from the location connected with the data signal line by which said two or more drain wires correspond, and the part which keeps away from said viewing area and is prolonged are a active-matrix mold display according to claim 5 to 7 characterized by having extended in the same direction substantially.

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DETAILED DESCRIPTION

[Detailed Description of the Invention]

[0001]

[Field of the Invention] This invention relates to the structure of the drain wire of a active-matrix display of choosing the drain wire arranged for every train, and giving a signal.

[0002]

[Description of the Prior Art] Current and the indicating equipment used are roughly divided and can be classified into a passive matrix mold and a active-matrix mold. among these, a active-matrix mold indicating equipment is an indicating equipment of the type which prepares a switching element in each pixel and displays by impressing the electrical potential difference according to the image data of the pixel to each pixel (or a current -- passing).

[0003] A liquid crystal display (Liquid Crystal Display;LCD) is an indicating equipment which displays by enclosing liquid crystal between the substrates which counter, impressing an electrical potential difference to the pixel electrode formed for every pixel, and changing the transmission of liquid crystal, and especially its active-matrix mold LCD is in use for a monitor application.

[0004] Moreover, an electroluminescence (Electro Luminescence;EL) display is a display which displays by passing a current to an EL element from the pixel electrode formed for every pixel, and research is prosperous in a active-matrix mold EL display towards utilization.

[0005] Drawing 4 is the circuit diagram showing the active-matrix mold LCD. Two or more drain wires 2 prolonged in the direction of a train and two or more gate lines 3 prolonged in a line writing direction are arranged, and the selection transistor 4 is arranged at the viewing area 1 corresponding to each intersection of a drain wire 2 and the gate line 3. The drain of the selection transistor 4 is connected to a drain wire 2, the gate is connected to the gate line 3, respectively, and the source is connected to the pixel electrode formed for every pixel. Above the viewing area 1, the drain wire selector 5 which chooses a predetermined drain wire, and six data signal lines 7 connected to the drain wire 2 through the drain wire selection transistor 6 are arranged. Beside the viewing area 1, the gate line selector 8 which chooses a gate line is arranged.

[0006] The gate line selector 8 makes sequential selection of the predetermined gate line 3 from two or more gate lines 3, impresses gate voltage, and turns on the selection transistor 4 connected to the gate line 3. The drain wire selector 5 makes sequential selection of the

predetermined drain wire 2 from two or more drain wires 2, and carries out sequential ON of the predetermined drain wire selection transistor 6. The drain wire 2 with which the drain wire selection transistor 6 became ON is connected with the corresponding data signal line 7, and a data signal is inputted into this drain wire 2. A data signal is impressed to the pixel electrode of a pixel connected to the selected gate line 3 and the selected drain wire 2 through a drain wire 2 and the turned-on selection transistor 4, the liquid crystal corresponding to this drives to it, and a display is performed to it.

[0007] Conventionally, the drain wire selector only made sequential selection of the one drain wire 2. However, the time amount from which the number of pixels becomes active [one drain wire] with an increment becomes short, since possibility that the response of liquid crystal stopped meeting the deadline arose, the number of the data signal line 7 is increased in recent years, and two or more drain wires 2 are activated more often at coincidence. Drawing 4 illustrated 6 layer structures which make the data signal line 7 a total of six [every two RGB], and activate six drain wires 2 at coincidence. The output of the drain wire selector 5 common to the gate electrode of the drain wire selection transistor 6 is impressed, and six except one of a right end of six drain wires 2 illustrated to drawing 2 are turned on in coincidence. Although omitted for simplification of a drawing, a right end drain wire is similarly turned on in five drain wires and coincidence which are not illustrated.

[0008] Although explanation is omitted, the multilayer structure of 12 layer structure and 24 layer structure which increased the data signal line 7 further also exists. Since many general more many layer structures, then time amount from which one drain wire 2 becomes active are securable, when the number of pixels increases further, for example, they have the request made into more layer structures.

[0009] Drawing 5 is the top view which expanded near the data signal line 7 and the drain wire selection transistor 6. The data signal line 7 is prolonged horizontally RGB each 2 6 color of every. It connected with the data signal line seven R1 through contact 11, and the 1st drain wire up wiring 10 has extended to the drain wire selection transistor 6. The drain wire selection transistor 6 has gate electrode 6a and barrier layer 6b. Gate electrode 6a is connected to the drain wire selector 5 by wiring which is not illustrated. The source of barrier layer 6b is connected to the 1st drain wire up wiring 10. It connected with the 1st drain wire lower wiring 12, and the drain of barrier layer 6b is prolonged to the viewing area 1. Drain wire up wiring and drain wire lower wiring are synthesized, and it is called a drain wire.

[0010] The 2nd drain wire up wiring 13 is connected to data signal line 7G1 through contact 14, it extends to the drain wire selection transistor 6, and the 2nd drain wire lower wiring 15 is connected to this.

[0011] Through contact 17, through contact 20, the 6th drain wire up wiring 25 is connected to data signal line 7 B-2 through contact 26, respectively, and the 3rd drain wire up wiring 16 is connected [the 4th drain wire up wiring 19] to data signal line 7G2 for the 5th drain

wire up wiring 22 like the following through contact 23 on the data signal line seven R2 at the data signal line seven B1.

[0012] In order that the drain wire up wiring 10, 13, 16, 19, 22, and 25 may arrange resistance mutually at this time, it is formed by the same quality of the material, the same line breadth, and the same die length. Since the data signal of a damping factor with which the damping factor of a data signal changes with each drain wires, and differ every drain wire 2 will be impressed if resistance of up wiring differs, this is for preventing that display quality deteriorates as a result.

[0013]

[Problem(s) to be Solved by the Invention] However, the problem described below arises in above-mentioned multilayer structure.

[0014] The 1st drain wire up wiring 10 is connected to R1 located in the maximum upper case among the data signal lines 7. On the other hand, the 6th drain wire up wiring 25 is connected to B-2 located in the re-lower berth among the data signal lines 7. Then, although the 1st drain wire up wiring 10 intersects five data signal lines 7 to which self is not connected, in the 6th drain wire up wiring 25, the data signal line 7 to which self is not connected does not cross.

[0015] At the crossing of wiring, if parasitic capacitance occurs and parasitic capacitance occurs, the imitation when changing the electrical potential difference impressed to wiring will become slow. Generally, the response to electrical-potential-difference change becomes slow, so that parasitic capacitance is large.

[0016] Therefore, with the 1st drain wire up wiring 10 and the 6th drain wire up wiring 25, since big parasitic capacitance occurs and a speed of response becomes slow so that more data signal lines 7 are intersected, since responsibility differs, the problem that display quality deteriorates arises.

[0017] If this considers as 12 layers, 24 layers, and further multilayer structure, it will appear more notably.

[0018] A difference does not produce the data signal line 7 in the signal delay for every drain wire as multilayer structure, but this invention aims at offering the high active-matrix mold display of display quality.

[0019]

[Means for Solving the Problem] The viewing area which accomplishes this invention in order to solve the above-mentioned technical problem and by which two or more pixel electrodes have been arranged, Two or more data signal lines arranged at the periphery of said viewing area, and two or more drain wires which are connected to any one of said two or more data signal lines, respectively, and extend to said viewing area, in the active-matrix mold display which has two or more gate lines which intersect said two or more drain wires, and extend in a viewing area said two or more drain wires It is the active-matrix mold display which extends so that at least one of data signal lines other than the data signal line to which the drain wire was connected may be intersected.

[0020] Furthermore, said all drain wires have the part which intersects all data signal lines other than the data signal line to which the drain wire was connected.

[0021] furthermore, the area of the part to which each of said drain wire intersects said data signal line -- said all drain wires -- setting -- parenchyma -- it is equal.

[0022] furthermore, the distance from the location connected with the data signal line by which the drain wire selection switching element for choosing said two or more drain wires as the position of the part prolonged toward said viewing area from the location connected with the data signal line by which said two or more drain wires correspond intervenes, and said two or more drain wires correspond to said drain wire selection switching element -- said two or more drain wires -- mutual -- parenchyma -- it is equal.

[0023] Moreover, the viewing area by which two or more pixel electrodes have been arranged and two or more data signal lines arranged in parallel mutually at the periphery of said viewing area, Two or more drain wires which are connected to any one of said data signal lines, respectively, and extend to a viewing area, Two or more gate lines which intersect said drain wire and extend to a viewing area, The switching element by which it is arranged corresponding to each intersection with said drain wire and said gate line, and the source is connected to said pixel electrode corresponding to said gate line in the gate corresponding to said drain wire in a drain, respectively, In the active-matrix mold display which **** said some of two or more drain wires [at least] The part prolonged toward said viewing area from the location connected with the corresponding data signal line, The sum of the area which has the part which keeps away from said viewing area and is prolonged, and intersects data signal lines other than the data signal line to which the drain wire was connected in each part, and the drain wire and data signal line in each crossing superimpose is equal at said each of two or more drain wires.

[0024] Furthermore, the part prolonged toward said viewing area from the location connected with the data signal line by which said two or more drain wires correspond, and the part which keeps away from said viewing area and is prolonged are the same sizes substantially, and the number with which said drain wire and said data signal line cross is equal at said each of two or more drain wires.

[0025] furthermore, the distance from the location connected with the data-signal line by which the drain signal selection switching element for choosing said two or more drain wires as the position of the part prolonged toward said viewing area from the location connected with the data signal line by which said two or more drain wires correspond intervenes, and two or more of said drain wires correspond to said drain signal selection switching element -- two or more of said drain wires -- mutual -- parenchyma -- it is equal.

[0026] Furthermore, the part prolonged toward said viewing area from the location connected with the data signal line by which said two or more drain wires correspond, and the part which keeps away from said viewing area and is prolonged are substantially prolonged in the same direction.

[0027]

[Embodiment of the Invention] As 1st operation gestalt of this invention, the case where this invention is applied to LCD is illustrated, and it explains below. Since the circuit diagram of this operation gestalt is completely the same as that of the conventional thing shown in drawing 4 and the same is said of the actuation, explanation is omitted.

[0028] Drawing 1 is the top view which expanded near the data signal line 7 and the drain wire selection transistor 6 of LCD concerning this operation gestalt.

[0029] The data signal line 7 is prolonged horizontally RGB each 2 6 color of every. It connected with the data signal line seven R1 through contact 51, and the 1st drain wire up wiring 50 has extended to the drain wire selection transistor 6. The drain wire selection transistor 6 has gate electrode 6a and barrier layer 6b. Gate electrode 6a is connected to the drain wire selector 5 by wiring which is not illustrated. The source of barrier layer 6b is connected to the 1st drain wire up wiring 50. It connected with the 1st drain wire lower wiring 52, and the drain of barrier layer 6b is prolonged to the viewing area 1.

[0030] The 2nd drain wire up wiring 53 is connected to data signal line 7G1 through contact 54, it extends to the drain wire selection transistor 6, and the 2nd drain wire lower wiring 55 is connected to this.

[0031] Through contact 57, through contact 60, the 6th drain wire up wiring 65 is connected to data signal line 7 B-2 through contact 66, respectively, and the 3rd drain wire up wiring 56 is connected [the 4th drain wire up wiring 59] to data signal line 7G2 for the 5th drain wire up wiring 62 like the following through contact 63 on the data signal line seven R2 at the data signal line seven B1.

[0032] In order that the drain wire up wiring 50, 53, 56, 59, 62, and 65 may arrange resistance mutually at this time, it is formed by the same quality of the material, the same line breadth, and the same die length.

[0033] A different point from the former of this operation gestalt is a point that the capacity lines 68, 69, 70, 71, and 72 are connected to the 2nd to 6th drain wire up wiring 53, 56, 59, 62, and 65. The capacity lines 68, 69, 70, 71, and 72 are made to call a capacity line the side further than contact on a data signal line from a viewing area here for the facilities of explanation, although it is formed in one with the drain wire up wiring 53, 56, 59, 62, and 65 and the boundary line does not exist. Since the 1st drain wire up wiring 50 is connected to the data signal line seven R1 of the maximum upper case and the data signal line 7 does not exist in a side far from a viewing area 1 rather than it, the capacity line is not formed.

[0034] By to which data signal line the drain wire is connected, as for a capacity line, die length differed, and from contact on a data signal line, all the capacity lines were prolonged toward the direction which keeps away from a viewing area, intersected the data signal line to which the drain wire is not connected, and have extended in the side far from a viewing area rather than the data signal line seven R1 of the maximum upper case. In this operation gestalt, the width of face of a capacity line is the same as drain wire up wiring.

[0035] By this, the sum totals of a count with which drain wire up wiring and a capacity line intersect the data signal line 7 are all drain wires, and become 5 times equally. Although the

parasitic capacitance which wiring makes is decided by area which wiring superimposes, since a capacity line and drain wire up wiring are the same line breadth, in this operation gestalt, the parasitism capacity value is only determined by the count of a crossover with a data signal line. Therefore, since the data signal line 7 and the sum totals of the capacity to form are all drain wires, drain wire up wiring and a capacity line become equal and responsibility differs for every drain wire, the problem that display quality deteriorates is solved.

[0036] Here, arrangement of a capacity line is explained. As mentioned above, it is necessary to make equal the resistance from the contact on a drain wire and a data signal line to the drain wire selection transistor 6. Therefore, drain wire up wiring is good [arrangement of a capacity line] like this operation gestalt to prepare so that it may extend in the opposite side rather than it makes it branch from somewhere in drain wire up wiring and arranges. Moreover, like branching of the capacity line mentioned above also in this case, although the line breadth of drain wire up wiring can be adjusted only at the crossing of drain wire up wiring and a data signal line and parasitic capacitance can also be adjusted, since resistance of drain wire up wiring changes, it cannot be said that it is the optimal. If it puts in another way, a capacity line does not contribute to transfer of a data signal, but is playing only a role of adjustment of capacity.

[0037] Moreover, a capacity line is good to lengthen in the same direction as drain wire up wiring. It is because intersectional superposition area differs and it becomes impossible to arrange parasitic capacitance even if line breadth is equal, when drain wire up wiring differs in a crossover include angle with the data signal line 7 from a capacity line.

[0038] By the way, with this operation gestalt, the distance from contact on drain wire up wiring and a data signal line to a drain wire selection transistor is all drain wires, and is equal. This is the treatment for being each drain wire and making equal the electric resistance of drain wire up wiring, as mentioned above. On the other hand, changing the size of drain wire up wiring mutually is proposed as an approach for arranging the electric resistance of drain wire up wiring from the former.

[0039] Drawing 2 is the top view of the active-matrix mold display into which the size of drain wire up wiring was changed. The drain wire up wiring 81 connected to the data signal line of the maximum upper case distant from a viewing area is the thickest, and the drain wire up wiring 86 which connects with the data signal line of the re-lower berth is formed most thinly. Since the resistivity of wiring will fall if the size of wiring becomes thick, resistance of all drain wire up wiring can be arranged by optimizing die length and a size.

[0040] If resistance is arranged by this approach, since the die length of drain wire up wiring can be shortened, there is a merit which can reduce the field of wiring slightly, but on the other hand at a crossing with the data signal line to which itself is not connected, the drain wire up wiring 81 connected to the maximum upper case has thick wiring, and its area superimposed on a data signal line is large. On the contrary, the drain wire up wiring 83 which intersects one data signal line does not intersect one in the top where wiring is thin.

Therefore, the difference of the parasitic capacitance of drain wire up wiring and a data signal line is expanded more.

[0041] Although a capacity line can be arranged also in this case according to the same idea and capacity can be arranged, a device is required for arrangement of a capacity line. The top view of the active-matrix mold display applied to the 2nd operation gestalt of this invention at drawing 3 is shown. As for the drain wire up wiring 81, 82, 83, 84, 85, and 86, according to the die length, line breadth differs like drawing 2. And the capacity lines 91, 92, 93, and 9495 are formed in the side far from those viewing areas 1. The width of face of these capacity line differs, respectively, and it is set up so that the sum of the area which the capacity line and corresponding drain wire up wiring superimpose at a crossing with the data signal line 7, respectively may become equal mutually.

[0042] The sum of the area which drain wire up wiring superimposes on a data signal line is short, and the area which a capacity line superimposes on a data signal line is each drain wire, and the place which this invention means should have it so that clearly from the 1st operation gestalt and the 2nd operation gestalt. [just equal] However, if the 1st operation gestalt is compared with the 2nd operation gestalt, the parasitic capacitance of drain wire up wiring and a data signal line is small, and since the responsibility of the whole drain wire is good, the direction of the 1st operation gestalt will be considered that the 1st operation gestalt is more suitable.

[0043] In addition, although each above-mentioned operation gestalt illustrated and explained LCD, it is not restricted to this and can be applied to EL indicating equipment and all active-matrix indicating equipments, such as an LED display equipment.

[0044]

[Effect of the Invention] Since it has the part to which a drain wire intersects data signal lines other than the data signal line to which itself was connected once [at least] according to this invention as explained in full detail above, the difference of the capacity for every drain wire is small, and the difference of the response time of each drain wire is small. Therefore, the difference of the signal delay for every drain wire also as multilayer structure is small, and can use the data signal line 7 as the high active-matrix mold display of display quality.

[0045] Furthermore, since it has the part to which all drain wires intersect all data signal lines other than the data signal line to which the drain wire was connected, the difference of the capacity for every drain wire is still smaller, and it can consider as a active-matrix mold display with still higher display quality.

[0046] Furthermore, the area of the part to which each of a drain wire intersects a data signal line is that which parenchyma etc. is by carrying out in all drain wires, and its difference of the capacity for every drain wire is still smaller, and it can be used as a active-matrix mold display with still higher display quality.

[0047] furthermore, to the position of the part prolonged toward a viewing area from the location connected with the data signal line by which two or more drain wires correspond

The drain wire selection switching element for choosing two or more drain wires intervenes. The distance from the location connected with the data signal line by which two or more drain wires correspond to a drain wire selection switching element By that which parenchyma etc. is by carrying out mutually with two or more drain wires, after suppressing the increment in the parasitic capacitance of a drain wire and a data signal line, resistance of drain wires can be arranged.

[0048] Moreover, the part prolonged toward said viewing area from the location connected with the data signal line by which some drain wires [at least] correspond, Have the part which keeps away from said viewing area and is prolonged, intersect the data signal line which does not correspond in each part, and since the superposition area of the drain wire in this crossing and a data signal line is up to drain wires and is equal The response time of each drain wire is equal, and a difference does not arise in the signal delay for every drain wire as multilayer structure, but it can use the data signal line 7 as the high active-matrix mold display of display quality.

[0049] Especially the part prolonged toward said viewing area from the location connected with the data signal line by which said two or more drain wires correspond and the part which keeps away from said viewing area and is prolonged The count which is the same size substantially and crosses in these parts It is up to said two or more drain wires, and since it was equal, after arranging the parasitic capacitance of each drain wire, the increment in capacity can be suppressed to the minimum, and can be used as the high active-matrix mold display of display quality with little signal delay.

[0050] furthermore, to the position of the part prolonged toward said viewing area from the location connected with the data signal line by which said two or more drain wires correspond The drain signal selection switching element for choosing said two or more drain wires intervenes. The distance from the location connected with the data signal line by which said two or more drain wires correspond to said drain signal selection switching element By that which parenchyma etc. is by carrying out mutually with said two or more drain wires, resistance of drain wires is equal and can consider as the high active-matrix mold display of display quality.

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DESCRIPTION OF DRAWINGS

[Brief Description of the Drawings]

[Drawing 1] It is the top view showing the active-matrix mold display concerning the 1st operation gestalt of this invention.

[Drawing 2] It is the top view of the conventional active-matrix mold display.

[Drawing 3] It is the top view showing the active-matrix mold display concerning the 2nd operation gestalt of this invention.

[Drawing 4] It is the circuit diagram showing a active-matrix mold display.

[Drawing 5] It is the top view of the conventional active-matrix mold display.

[Description of Notations]

2 Drain Wire

3 Gate Line

6 Drain Wire Selection Transistor

7 Data Signal Line

50, 53, 56, 59, 62, 65 Drain wire up wiring

68, 69, 70, 71, 72 Capacity line

91, 92, 93, 94, 95 Capacity line

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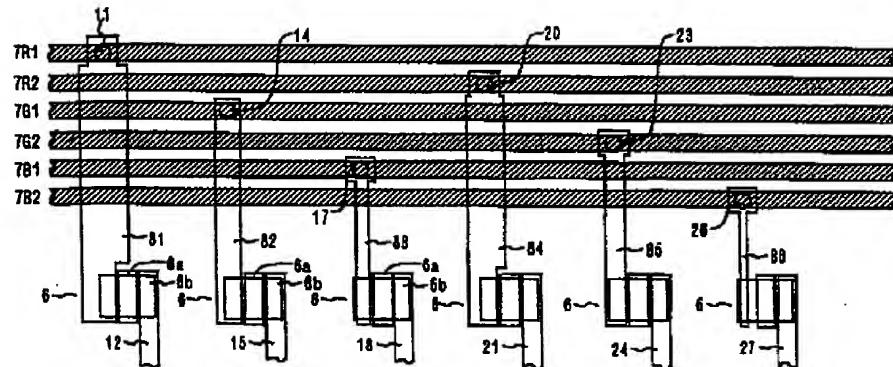
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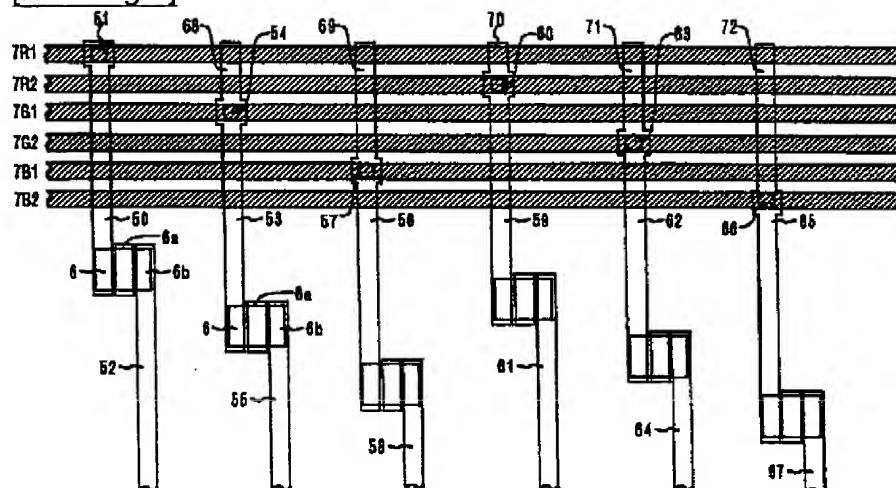
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DRAWINGS

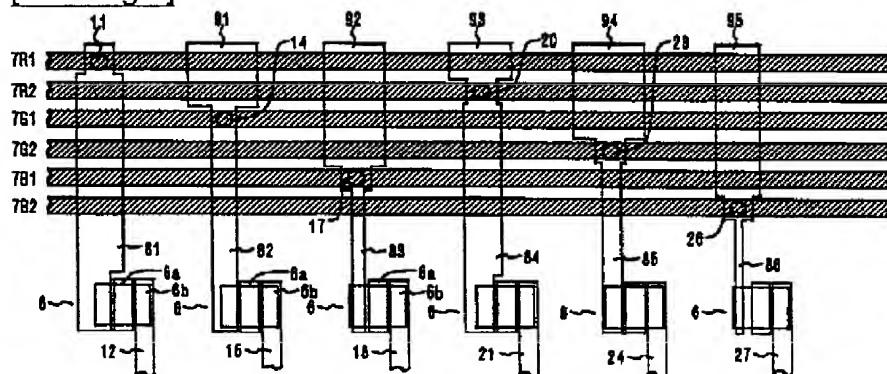
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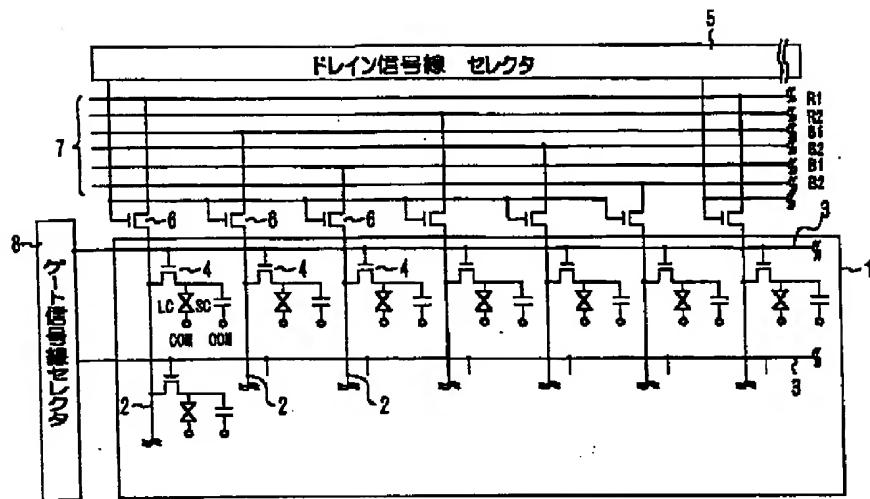
[Drawing 1]



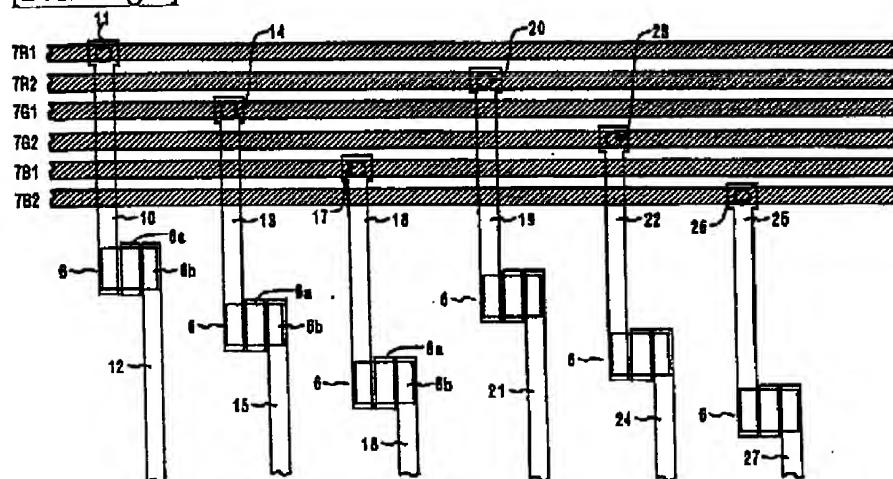
[Drawing 3]



[Drawing 4]



[Drawing 5]



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